REMARKS/ARGUMENTS

In this response, claims 1, 11, 17, and 20 are amended. No claims are canceled or added. Thus, after entry of this amendment, claims 1-22 remain pending.

Claim Rejections under § 103(a), Prior Art in view of Rinaldi

Claims 1-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over the admitted prior art (Fig. 1A, 1B, page 2, (0005)-(0006)) in view of Rinaldi et al (US Patent No. 6,327,002 B1).

Claims 1-10

Claim 1 is allowable as Rinaldi does not teach or suggest each and every element of claim 1. For example, claim 1 recites:

> *an encoder coupled to an output of the pixel pipeline circuit and having one or more processor elements configured to convert the pixel stream to digital sample values corresponding to a target analog signal representing the pixel stream in the target format, thereby generating a base data stream at a base sampling rate corresponding to the target format;*
>
> *a supersampling circuit coupled to an output of the encoder and configured to generate a supersampled data stream at a supersampling rate from the base data stream, the supersampling rate being higher than the base sampling rate; and*
>
> *a digital to analog converter coupled to an output of the supersampling circuit and configured to convert the supersampled data stream to the analog output signal having the target format with the base sampling rate.*

At page 2, the Office Action states that the upsampling circuit 70 of Rinaldi would be put after the encoder 134 of FIG. 1B to produce a plurality of different video outputs. It is presumed that the desired video output is asserted to be the analog output signal of claim 1.

Below, I talk about three rates R1-R3. R2 is the rate for the analog output signal. R1 is less than R2, and R3 is greater than R2.

Proposed Combination

At page 4, the Office Action states that "Rinaldi et al teach that the up sampling module 70 which changes the sampling frequency of the signals to match the desired output sampling frequencies (Fig. 2, col. 3, line 35 to col. 4, line 16)." (emphasis added). An output signal having the desired output sampling frequency is then output from the DAC 23 as outputs

30 or 32. *Id.*, FIG. 2. Thus, the upsampling module 70 receives an input signal at a rate R1 and outputs a signal at rate R2, which matches the output frequency. The DAC 23 then receives the analog signal at R2 and outputs the digital signals 30 and 32 at R2, which is the desired output frequency.

Accordingly, in order to produce the desired video output, the encoder 134 would output a signal at the rate R1, the upsampling module would convert the input at R1 to an output signal at R2, and the DAC 23 would output an analog signal at R2.

A. Proposed encoder outputs signal at R1, not at R2

As described above, the proposed encoder outputs a signal at R1, which needs to be converted to R2 in order to obtain the desired video output format.

In contrast, claim 1 recites "*[a] device for converting a digital pixel signal to an analog output signal having a target format.*" Thus, the analog output signal has a target format. Claim 1 also recites that the encoder outputs "*digital sample values corresponding to a target analog signal representing the pixel stream in the target format.*" Therefore, the encoder outputs a signal in the same format as the eventual analog output signal, which is at the rate R2 that is *"a base sampling rate corresponding to the target format.*"

As the proposed combination teaches an encoder outputting a signal at a rate of R1, which is below the output rate R2, the proposed combination does not teach or suggest an encoder outputting a signal "*in the target format,*" i.e. R2, as recited in claim 1.

B. Supersampling circuit increases rate from R2 to R3, not R1 to R2.

As described above, the output of the claimed encoder is at a rate of R2 (i.e. the base sampling rate). Claim 1 recites that "*the supersampling rate [is] higher than the base sampling rate*" R2. Thus, the supersampling rate is R3, which is higher than R2. Since the upsampling module 70 increases the rate from R1 to R2, and not R2 to R3, the proposed combination does not teach or suggest this claim element.

C. DAC 23 keeps rate constant at R2, and does not convert from R3 to R2

As described above, the DAC 23 of the proposed combination receives a digital signal at R2 and outputs analog signals 30 and 32 at the desired output sampling frequencies R2.

Thus, the DAC 23 keeps the rate at R2, although it does convert from a digital representation to an analog representation.

In contrast, claim 1 recites that the DAC is configured to "*convert the supersampled data stream [at R3] to the analog output signal having the target format with the base sampling rate*," which is the same rate R2 output from the encoder. Since the DAC receives and outputs signals at the same rate R2, the proposed combination does not teach this claim element.

D. Asserted process is digital R1-> digital R2->analog R2, not R2->R3->R2.

The proposed method of the combination and the function of the upsampling module 70 are fundamentally different from the functionality of claim 1.

The proposed combination converts from a lower rate R1 to the output rate R2 so that different (e.g. higher) video formats could be achieved. Thus, the conversion is only from R1->R2.

In contrast, claim 1 recites a process where a rate of a signal is brought higher and then brought down to a lower rate. Thus, regardless of the labels of the rates, the conversion process would be from a lower rate -> a higher rate -> a lower rate. The proposed combination does not have this last step of going from a higher rate to a lower rate.

As shown in FIG. 4A-4C, echoes are suppressed by implementing this last step. Note that this last step is possible since the signal from the encoder to the DAC has been upsampled to the higher rate by the supersampling circuit..

For at least these reasons, claim 1 and its dependent claims are allowable over the admitted prior art and Rinaldi.

Claims 11-22

Applicants submit that independent claim 11, and its dependent claims 12-16; independent claim 17, and its dependent claims 18-19; and independent claim 20, and its dependent claims 21-22, are allowable for at least some of the same reasons as claim 1.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance and an action to that end is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 415-576-0200.

Respectfully submitted,

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